IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Carl Christensen et al. Examiner: Michael C. Colucci

Serial No: 10/519,000 Group Art Unit: 2626

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For: BROADCAST ROUTER HAVING A SERIAL DIGITAL AUDIO DATA STREAM DECODER

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Hon. Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

Applicants appeal the status of claims 1–24 as rejected in the final Office Action dated June 19, 2009 and the Advisory Action dated October 20, 2009, pursuant to the Notice of Appeal filed on November 3, 2009 and submit this appeal brief.

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1. Real Party in Interest

The real party in interest is THOMSON LICENSING S.A., the assignee of the entire right title and interest in and to the subject application by virtue of an assignment from the inventors recorded with the Patent Office on 12/21/2004 at reel/frame 016551/0479.

2. **Related Appeals and Interferences**

None.

3. Status of claims

claims 1–24 are pending. claims 1–24 stand rejected and are under appeal.

A copy of the claims 1–24 is presented in Section 8 below.

4. Status of Amendments

An amendment was filed under 37 C.F.R. § 1.111 in response to the Non-final Office Action dated January 8, 2009. A response was filed under 37 C.F.R. § 1.116 to the Final Office Action dated June 16, 2009, but no amendment to the claims was made at that time. As such, the claims stand as amended in response to the Non-final Office Action of January 8, 2009.

5. <u>Summary of claimed Subject Matter</u>

Independent claim 1 is directed to "[a] method of extracting digital audio data words from a serialized stream of digital audio data" (claim 1, preamable).

The subject matter of the first element (beginning with "constructing") recited in claim 1 is described, e.g., at: page 1, lines 30–31 and page 14, lines 3–22.

The subject matter of the second element (beginning with "extracting") recited in claim 1 is described, e.g., at: page 1, line 31 through page 2, line 2, page 14, lines 16–22, and page 18, line 17 through page 19, line 31.

The subject matter of the third element (beginning with "each one of said extracted plural digital audio data words") recited in claim 1 is described, e.g., at: page 15, line 23 through page 16, line 6.

The subject matter of the fourth element (beginning with "wherein said bit time") recited in claim 1 is described, e.g., at: page 12, lines 6–18 and FIG. 5.

Independent claim 11 is directed to "[a] method of extracting digital audio data words from a serialized stream of digital audio data" (claim 1, preamble).

The subject matter of the first element (beginning with "constructing") recited in claim 11 is described, e.g., at: page 1, lines 30–31 and page 14, lines 3–22.

The subject matter of the second element (beginning with "sampling") recited in claim 11 is described, e.g., at: page 10, lines 12–14.

The subject matter of the third element (beginning with "extracting") recited in claim 11 is described, e.g., at: page 1, line 31 through page 2, line 2, page 14, lines 16–22, and page 18, line 17 through page 19, line 31.

The subject matter of the fourth element (beginning with "wherein said bit time") recited in claim 11 is described, e.g., at: page 12, lines 6–18 and FIG. 5.

Independent claim 20 is directed to "[a] bi-phase decoder for use in decoding a stream of AES-3 digital audio data" (claim 20, preamble).

The subject matter of the first element (beginning with "a decoder circuit") recited in claim 20 is described, e.g., at: page 10, lines 12–17 and FIG. 4, element 298.

The subject matter of the second element (beginning with "a data store") recited in claim 20 is described, e.g., at: page 10, lines 23–26 and FIG. 4, element 302.

The subject matter of the third element (beginning with "said decoder circuit extracting") recited in claim 20 is described, e.g., at: page 11, line 20 through page 12, line 22 and page 14, line 23 through page 15, line 1.

The subject matter of the fourth element (beginning with "wherein said bit time") recited in claim 20 is described, e.g., at: page 12, lines 6–18 and FIG. 5.

Independent claim 23 is directed to "[a] method of extracting digital audio data words from a serialized stream of digital audio data" (claim 23, preamble).

The subject matter of the first element (beginning with "constructing") recited in claim 23 is described, e.g., at: page 1, lines 30–31 and page 14, lines 3–22.

The subject matter of the second element (beginning with "extracting") recited in claim 23 is described, e.g., at: page 1, line 31 through page 2, line 2, page 14, lines 16–22, and page 18, line 17 through page 19, line 31.

The subject matter of the third element (beginning with "each one of said extracted plural digital audio data words") recited in claim 23 is described, e.g., at: page 15, line 23 through page 16, line 6.

The subject matter of the fourth element (beginning with "estimating") recited in claim 23 is described, e.g., at: page 11, line 20 through page 12, line 3.

The subject matter of the fifth element (beginning with "constructing a bit window") recited in claim 23 is described, e.g., at: page 11, line 20 through page 12, line 3.

The subject matter of the sixth element (beginning with "identifying") recited in claim 23 is described, e.g., at: page 12, lines 6–18 and FIG. 5.

Independent claim 24 is directed to "[a] method of extracting digital audio data words from a serialized stream of digital audio data" (claim 24, preamble).

The subject matter of the first element (beginning with "constructing") recited in claim 24 is described, e.g., at: page 1, lines 30–31 and page 14, lines 3–22.

The subject matter of the second element (beginning with "sampling") recited in claim 24 is described, e.g., at: page 10, lines 12–14.

The subject matter of the third element (beginning with "extracting") recited in claim 24 is described, e.g., at: page 1, line 31 through page 2, line 2, page 14, lines 16–22, and page 18, line 17 through page 19, line 31.

The subject matter of the fourth element (beginning with "estimating") recited in claim 24 is described, e.g., at: page 11, line 20 through page 12, line 3.

The subject matter of the fifth element (beginning with "constructing a bit window") recited in claim 24 is described, e.g., at: page 11, line 20 through page 12, line 3.

The subject matter of the sixth element (beginning with "identifying") recited in claim 24 is described, e.g., at: page 12, lines 6–18 and FIG. 5.

The subject matter of the seventh element (beginning with "determining") recited in claim 24 is described, e.g., at: page 12, lines 4–22.

6. Grounds of Rejection to be Reviewed on Appeal

claims 1–24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over International Patent Publication WO 08/16040 to Adams (hereinafter "Adams") in view of U.S. Patent No. 5,956,674 to Smyth (hereinafter "Smyth") and in further view of European Patent Publication No. 0453063 to Fletcher (hereinafter "Fletcher"). This rejection is presented for review in this Appeal with respect to claims 1–24, as argued with respect to independent claims 1, 11, 20, 23, and 24 as well as certain dependent claims.

Regarding the grouping of the claims with respect to the rejection under 35 U.S.C. §103(a) 1–24, claims 2–10, 12–19, and 21–22 stand or fall with claims 1, 11, and 20 respectively due to their respective dependencies.

Additionally, claims 9–10, 19, 23, and 24 are argued separately. claim 10 stands or falls with claim 9 due to its dependency therefrom.

7. Argument

A. Introduction

In general, the present invention is directed to a broadcast router having a serial digital audio data stream decoder cross reference (Applicant's Specification, Title). As disclosed in the Applicant's specification at page 2, lines 4-20:

> Traditionally, serial digital audio decoders have used a PLL to lock to the incoming signal. However, in order to use a PLL in a serial digital audio decoder, various external components are typically required. As a result, serial digital audio decoders which incorporate a PLL tend to be both expensive and unwieldy. Furthermore, PLLs cannot readily be switched between manufacturing technologies. As a result, PLLs are not particularly well suited for use in devices which integrate plural design technologies, for example, different FPGA families and/or different standard cell and gate array families.

Advantageously, the present principles provide a decoder and methods for extracting digital audio data words from a serialized stream of digital audio data. The claims of the pending invention include novel features not shown in the cited references which have already been pointed out to the Examiner. These features provide advantages over the prior art and dispense with prior art problems such as those described above with reference to the background discussion in Applicant's specification.

Applicants respectfully assert that independent claims 1, 11, 20, 23, and 24 are each patentably distinct and non-obvious over the cited references in their own right. For example, the below-identified features of independent claims 1, 11, 20, 23, and 24 are not shown in any of the cited references, either taken singly or in any combination. Moreover, these claims are distinct from each other in that they are directed to different implementations and/or include different elements. Accordingly, each of independent claims 1, 11, 20, 23, and 24 represent separate features/implementations of the invention that are separately novel and non-obvious with respect to the prior art and to the other claims. As such, independent claims 1, 11, 20, 23, and 24 are separately patentable and are each presented for review in this appeal.

B. Whether claims 1–24 are Unpatentable Under 35 U.S.C. §103(a) With Respect To International Patent Publication WO 08/16040 to Adams in View of U.S. Patent No. 5,956,674 to Smyth and Further in View of European Patent Publication No. 0453063 to Fletcher

The failure of an asserted combination to teach or suggest each and every feature of a claim remains fatal to an obviousness rejection under 35 U.S.C. § 103. Section 2143.03 of the MPEP requires the "consideration" of every claim feature in an obviousness determination. To render a claim unpatentable, however, the Office must do more than merely "consider" each and every feature for this claim. Instead, the asserted combination of the patents must also teach or suggest *each and every claim feature*. *See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) (emphasis added) (to establish *prima facie* obviousness of a claimed invention, all the claim features must be taught or suggested by the prior art). Indeed, as the Board of Patent Appeal and Interferences has recently confirmed, a proper obviousness determination requires that an Examiner make "a searching comparison of the claimed invention - *including all its features* - with the teaching of the prior art." *See In re Wada and Murphy*, Appeal 2007-3733, *citing In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis in original). "If an independent claim is non-obvious under 35 U.S.C. 103, then any claim depending therefrom is non-obvious." MPEP §2143.03, *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Examiner has rejected claims 1–24 as being unpatentable over International Patent Publication WO 08/16040 to Adams (hereinafter "Adams") in view of U.S. Patent No. 5,956,674 to Smyth (hereinafter "Smyth") and further in view of European Patent Publication No. 0453063 to Fletcher (hereinafter "Fletcher"). The Examiner contends that the cited combination shows all the features recited in claim 1–24.

The Adams reference concerns a "method and apparatus for decoding of SPDIF or AES/EBU digital audio data" (Adams, Title). In further detail, Adams discloses the following in its Abstract:

> A circuit for decoding an input signal includes a measurement circuit having an input to receive a timing clock signal that is asynchronous with clocking of the input signal, to measure duration of a plurality of pulses received on the input signal in relation to frequency of the timing clock signal and a decode circuit to decode the input signal into digital data. In one embodiment, the circuit may include a servo mechanism for generating the timing clock signal to have a frequency that varies in response to variations in frequency of clocking of data on the input signal. The servo mechanism may include a digitally controlled oscillator and a feedback circuit, to control the digital frequency of the digitally controlled oscillator in response to variation of clocking of data on the input signal. The invention permits use of all digital components for decoding digital audio data encoding using biphase-mark encoded data according to the SPDIF or AES/EBU standards.

Smyth concerns a "multi-channel predictive subband audio coder using psychoacoustic adaptive bit allocation in frequency, time and over multiple channels" (Smyth, Title). In further detail, Smyth discloses the following in its Abstract:

> A subband audio coder employs perfect/non-perfect reconstruction filters, predictive/non-predictive subband encoding, transient analysis, and psycho-acoustic/minimum mean-square-error (mmse) bit allocation over time, frequency and the multiple audio channels to encode/decode a data stream to generate high fidelity reconstructed audio. The audio coder windows the multi-channel audio signal such that the frame size, i.e. number of bytes, is constrained to lie in a desired range, and formats the encoded data so that the individual subframes can be played back as they are received thereby reducing latency. Furthermore, the audio coder processes the baseband portion (0–24 kHz) of the audio bandwidth for sampling frequencies of 48 kHz and higher with the same encoding/decoding algorithm so that audio coder architecture is future compatible.

Fletcher concerns a technique for "decoding biphase signals by measuring pulse lengths" (Fletcher, Title). In further detail, Adams discloses the following in its Abstract:

> A biphase-mark coded digital audio signal comprising short and long pulses (IEC) 958) is decoded despite substantial variation of sample rate but without a separate synchronization or timing signal and without a phase locked loop. The pulse lengths are measured (14) and then compared (22,20) with two thresholds. One (22) is a variable threshold derived by a generator (26) as 1.5 times the average length of the short pulses, this average being stored in register (28). This will normally be adequate to discriminate the short and long pulses. The second comparison (20) is with a fixed value with is lower than 1.5 times the pulse length at the highest input

frequency. When the comparators disagree irreconcilably in their determination, the resultant of the second comparison is used instead of the first. This allows the system to respond quickly to start-up or sudden change in input data rate.

As will be discussed further, the cited references do not teach or suggest all the features of claims 1–24 reproduced herein, thus warranting allowance of these claims.

B1. Claims 1–24

Initially, applicants point out that claims 2–10 directly or indirectly depend from independent claim 1, claims 12–19 directly or indirectly depend from independent claim 11, and claims 21–22 directly or indirectly depend from independent claim 20. Thus, claims 2–10 incorporate by reference include all of the elements of claim 1, claims 12–19 incorporate all of the elements of claim 11, and claims 21–22 incorporate by reference all of the elements of claim 20.

Further, applicants point out that claim 1, and dependent claims 2-10 include the feature "wherein … the time separating a first set of successive identified transitions is a first measurement of said estimated bit time." Claim 11 and 20 –24 recite the same language.

The Examiner asserts that Adams teaches this element, but the Examiner only makes general reference to biphase encoding. The Examiner has not pointed to any specific reference in Adams which describes *measurement* of an estimated bit time. Generally speaking, if a device does not know the bit time of a transmission, the device must estimate that bit time from the transmission itself. Applicants' claims present one technique for doing so, whereas Adams presents a different approach. In response to this argument, the Examiner merely cites the general features of biphase decoding without addressing the actual elements of applicants' claims.

How applicants measure the *first* estimated bit time has particular relevance, because little to no information exists at the decoder at that point in time. Applicants' invention uses the *measured* time between the first transitions to estimate the bit time, whereas Adams uses an assumed initial frequency.

Adams describes a technique for parsing the pulse lengths of a biphase data stream on page 8. Adams sets three taps to a signal at half-multiples of a time T, defined as "the period of

time for one cell in the biphase-mark encoded data input." (Adams, p. 8, lines 11–12). Adams adjusts the time T by adjusting the shift register's clock frequency. (Adams, p. 9, lines 9–12). Adams does this using a servo loop that performs continual adjustments, slowly increasing the frequency when processing data, and quickly dropping the frequency when a preamble is detected. (Adams, pp. 9–11). In particular, Adams describes how the circuit initially responds, giving examples of an initial frequency (and hence, an initial bit time) which is too high, and an initial frequency which is too low. (Adams, p. 11, lines 1–13). *Adams does not describe any means for determining the initial frequency*, nor for determining an initial time T. In the absence of any such description, Adams presumably relies on the prior art technique described in the patent for selecting an initial frequency, a technique based upon the known frequency of the input signal. (Adams, p. 5, lines 18–24).

The Examiner has not contradicted this analysis. Instead the Examiner has asserted that, "Adams explicitly teaches a period of time detected between transitions within a frame of AES biphase data, wherein this time is the time of incoming bits i.e. bit time." (Office Action of 1/8/09, p. 5, citing Adams, p. 8, lines 1–21). The cited portion of Adams relied upon by the examiner shows that different cells may be characterized as being .5T, 1T, or 1.5T in length. The Examiner relies on this teaching to assert that Adams detects a period of time between transitions.

However, Adams does not *make a first measurement of the estimated bit time*. The cited portion of Adams *uses a bit time* (T) to make its measurement. The bit time undergoes adjustment, as noted above, by changing the clock frequency. This passage fails, as does every other passage in Adams, to describe any new method for producing an initial frequency, and hence an *initial* bit time. As noted above, Adams uses the prior art method of determining this quantity that is set forth in its description of the prior art. (Adams, p. 5, lines 18–24).

Adams does not *measure* the time between the first transitions in order to estimate bit time. Instead, Adams merely uses a standard frequency to determine its initial bit time. Subsequent detection of bits occurs based on the bit time and cannot represent a *first measurement* of the bit time. The Examiner has perhaps been misled by the apparent similarities between Adams and the present invention, but ultimately the Examiner must account for *every* element in applicants' claims.

Applicants respectfully assert that Adams does not disclose or suggest that a first measurement for an estimated bit time constitutes the time separating a first set of successive identified transitions.

Fletcher fails to cure the deficiencies of Adams. Fletcher's estimation of bit times is unreliable initially. (Fletcher, Col. 3, lines 30–52.) Fletcher teaches setting an initial value for its average bit time to be zero. (Fletcher, Col. 3, lines 32–34.) Because this results in poor behavior initially, Fletcher has a fixed threshold comparator (20) which essentially sets a minimum bit time that is roughly equal to the shortest expected pulse. (Fletcher, Col. 3, lines 47–50.) This threshold allows Fletcher's technique to function while its average builds up from the initial value of zero, but ultimately decreases the flexibility as it sets a hard limit on the system's functional sampling rate, beyond which the threshold would improperly interpret all pulse lengths as "A" pulses.

Fletcher explicitly states that the first measurement for its average, and hence for its estimated bit time, is *zero*. Therefore, applicants assert that Fletcher fails to disclose or suggest a first measurement for an estimated bit time corresponding to the time separating a first set of successive identified transitions.

Smyth fails to cure the deficiencies of Adams and Fletcher. The Examiner describes Smyth at length, but does not set forth any way in which Smyth makes an estimate of bit time. Smyth does not concern itself at all with biphase encoding, and as such, the need to estimate a bit time does not arise. Therefore, neither Adams, Smyth, nor Fletcher, taken singly or in any combination, teach the all the elements recited in applicants' claims 1–24.

Accordingly, claims 1–24 patentably distinguish over Adams, Smyth, and Fletcher for at least the reasons set forth above. Therefore, applicants request reversal of the rejection of claims 1–24.

B2. Claims 9–10, 19, 23, and 24

Claim 10 directly depends from claim 9 and incorporates by reference all the elements of claim 9. Claims 9–10 include the feature of "estimating minimum and maximum bit window times." Claims 19, 23, and 24 recite the same language. The Examiner asserts that the Adams

reference discloses this feature in its discussion of the shift register and FIG. 11. The Examiner goes on to argue that Smyth teaches "windows." In the Advisory Action the Examiner reaffirms this argument, but does so only by, again, noting general similarities between the present invention and Adams.

However, the Examiner has not shown that either Adams or Smyth discloses or suggests *estimating* minimum and maximum bit window times. Simply showing that a window has a maximum and a minimum time is insufficient to read on applicants' claimed feature. Adam's shift register serves to discriminate between different pulse lengths. Adams makes use of delay taps, with the delay length based on a continually adjusting servo loop. These taps do not constitute minimum or maximum bit window times, and therefore Adams does not estimate such bit window times.

In contrast, the present invention constructs a timing window based on an estimated bit time. In order to estimate a bit time, applicants estimate a bit window, for example as described in their application at pages 11 and 12. The bit window and timing window constitute *ranges* which represent different quantities. Adams does not have any analogue for bit window times. Rather, as noted above, Adams determines a bit time T by a different mechanism. As such, Adams never discloses or suggests *estimating* bit window times.

Smyth cannot cure this deficiency. The Examiner states, "Smyth has been incorporated to further teach … the use of largest and smallest bit window times." (Final Office Action of 6/19/09, pp. 7–8, bridging paragraph). The Examiner then describes how Smyth selects a window size. However, applicants note that Smyth's window does not constitute the equivalent of a "segment from a data stream which contains the data of interest" that the Examiner suggests. *Id.* Instead, "window size" in the context of Smyth refers to a number of PCM samples that go into a particular frame. Smyth's window does not constitute a range which contains an important quantity, but simply represents a determination of how large a frame will be. (*See* Smyth, Col. 5, lines 52–67). As a result, Smyth clearly does not disclose or suggest estimating window times at all.

Even assuming, *arguendo*, that the Examiner's interpretation of Smyth were reasonable, Smyth fails to show an estimation. The difference between a *selection* and an *estimation* is of particular importance here. Smyth selects a window size to optimize performance. Smyth

thereby chooses the bounds of its window in order to tune the size of its frames. In contrast, the applicants *estimate* minimum and maximum bit window times. These are not quantities which are selected, but instead represent guesses at the range over which incoming bits might arrive. The difference between these two approaches is stark. Smyth selects a window time so that the frames it produces behave in a certain way, while applicants estimate a bit window time so to better detect incoming data. In Smyth, everything is under the system's control or may be reacted to in a fixed way (i.e., if the compression rate changes, the window may be increased). In the present invention, the incoming bit times are not within the system's control and must be estimated as they arrive.

Applicants respectfully assert that Smyth fails to disclose or suggest *estimating* maximum and minimum bit window times.

Fletcher fails to cure the deficiencies of Adams and Smyth in this respect. Fletcher's technique for estimating bit times does not rely on bit windows, but instead builds a bit time estimate progressively with the average. Because Fletcher takes an alternate approach for estimating bit times, Fletcher has no need for *bit window times*, and therefore Fletcher does not disclose or suggest estimating minimum or maximum bit window times.

Fletcher, and/or Smyth, taken alone or in any combination, fail to disclose or suggest estimating minimum or maximum bit window times.

Further, claims 9–10 recite, inter alia, "constructing a bit window from said minimum and maximum bit window times." Claims 19, 23, and 24 recite the same language. The Examiner asserts that these elements are disclosed by Adams in its summary.

The portion of Adams relied upon by the Examiner refers to "a coding scheme having a maximum pulse width." However, this section simply describes the general structure of biphase encoded data and says nothing regarding constructing a bit window, whether from minimum or maximum bit window times, or from any other value. Furthermore, as noted above, Adams determines its time T by a different mechanism from the applicants' invention and, as such, Adams never discloses or suggests estimating minimum or maximum bit window times. Adams also fails to disclose or suggest constructing a bit window from these minimum and maximum bit window times.

Presumably the Examiner again relies on Smyth to teach this element. However, as noted

above, Smyth does not disclose or suggest bit window times, and further does not disclose or suggest *estimating* bit window times, and hence does not use the recited minimum and maximum. Even if it did so, however, Smyth clearly does not disclose or suggest constructing a window from a minimum and maximum time.

Instead, Smyth describes only a "window size." As noted above, the window size of Smyth constitutes simply a number of samples which do not in any way describe a range. Smyth contains no indication whatsoever that this size depends upon a known maximum and minimum, as Smyth's window size is a simple integer (i.e., 256, 512…). Smyth describes only a single quantity — the size — which Smyth changes as needed based on such factors as compression. Therefore, Smyth does not disclose or suggest constructing a bit window from minimum and maximum bit window times.

Again, Fletcher fails to cure the deficiencies of Adams. Because Fletcher takes an alternate approach for estimating bit times, as noted above Fletcher has no need bit window times, and therefore it is respectfully asserted that Fletcher does not disclose or suggest constructing a bit window.

For at least the above reasons, claims 9–10, 19, 23, and 24 patentably distinguish over Adams, Smyth, and Fletcher for at least the reasons set forth above. Therefore, applicants' request reversal of the rejection claims 9–10, 19, 23, and 24.

E. Conclusion

The cited references do not disclose or suggest all of the features of the pending claims. Accordingly, applicants respectfully request that the Board reverse the rejections of claim 1–24 under 35 U.S.C. §103(a).

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Respectfully submitted,

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8. CLAIMS APPENDIX

1. (Rejected) A method of extracting digital audio data words from a serialized stream of digital audio data, comprising:

constructing a timing window from an estimated bit time for said serialized stream of digital audio data, said timing window having a preamble sub-window and at least one data sub-window;

extracting plural digital audio data words from said serialized stream of digital audio based upon the location of each transition in said serialized stream of digital audio data relative to said preamble sub-window and said at least one data sub-window of said timing window;

each one of said extracted plural digital audio data words having a preamble identifiable by a combination of at least one transition located in said preamble sub-window of said timing window and at least one transition located in said at least one data sub-window of said timing window;

wherein said bit time is estimated by averaging a plurality of data stream pulse lengths and the time separating a first set of successive identified transitions is a first measurement of said estimated bit time.

2. (Rejected) The method of claim 1, and further comprising identifying said extracted data words as having a first type of preamble if said extracted data words have a pair of successive transitions located in said preamble sub-window followed by a pair of successive transitions located in said at least one data sub-window.

3. (Rejected) The method of claim 2, and further comprising identifying said extracted data words as having a second type of preamble if said extracted data words have a pair of non-successive transitions located in said preamble sub-window-separated by a pair of successive transitions located in said at least one data sub-window.

4. (Rejected) The method of claim 3, and further comprising identifying said extracted data words as having a third type of preamble if said extracted data words have a transition located in said preamble sub-window followed by first, second and third transitions located in said at least one data sub-window.

5. (Rejected) The method of claim 4, wherein said timing window is constructed such that said preamble sub-window extends from about 1¼ times said estimated bit time to about 1¾ times said estimated bit time.

6. (Rejected) The method of claim 5, wherein said timing window is constructed such that said at least one data sub-window extends from about ¼ times said estimated bit time to about 1¼ times said estimated bit time.

7. (Rejected) The method of claim 4, wherein said timing window is constructed such that said at least one data sub-window includes a first data sub-window which extends from about ¼ times said estimated bit time to about ¾ times said estimated bit time and a second data sub-window which extends from about ¾ times said estimated bit time to about 1¼ times said estimated bit time.

8. (Rejected) The method of claim 1, wherein said estimated bit time is derived from said serialized stream of digital audio data.

9. (Rejected) The method of claim 8, and further comprising:

estimating minimum and maximum bit window times;

constructing a bit window from said minimum and maximum bit window times;

identifying transitions in said serialized stream of digital audio data which occur within said constructed bit window.

10. (Rejected) The method of claim 9, and further comprising determining said estimated bit time from a running average of plural measurements of said estimated bit time.

11. (Rejected) A method of extracting digital audio data words from a serialized stream of digital audio data, comprising:

constructing a timing window from an estimated bit time for said serialized stream of digital audio data, said timing window having a preamble sub-window and at least one data sub-window;

sampling said serialized stream of digital audio data at a fast sample rate; and

extracting plural digital audio data words from said serialized stream of digital audio based upon the location of each transition in said sampled stream of digital audio data relative to said preamble sub-window and said at least one data sub-window of said timing window;

wherein said bit time is estimated by averaging a plurality of data stream pulse lengths and the time separating a first set of successive identified transitions is a first measurement of said estimated bit time.

12. (Rejected) The method of claim 11, wherein said fast sample rate is at least about twenty times faster than a data rate for said serialized stream of digital audio data.

13. (Rejected) The method of claim 12, wherein said fast sample rate is derived from a fast clock having a frequency of at least about twenty times faster than the frequency of said serialized stream of digital data.

14. (Rejected) The method of claim 13, wherein each one of said extracted plural digital audio data words has a preamble identifiable by a combination of at least one transition located in said preamble sub-window of said timing window and at least one transition located in said at least one data sub-window of said timing window.

15. (Rejected) The method of claim 14, and further comprising identifying said extracted data words as having a first type of preamble if said extracted data words have a pair of successive transitions located in said preamble sub-window followed by a pair of successive transitions located in said at least one data sub-window.

16. (Rejected) The method of claim 15, and further comprising identifying said extracted data words as having a second type of preamble if said extracted data words have a pair of non-successive transitions located in said preamble sub-window separated by a pair of successive transitions located in said at least one data sub-window.

17. (Rejected) The method of claim 16, and further comprising identifying said extracted data words as having a third type of preamble if said extracted data words have a transition located in said preamble sub-window followed by first, second and third transitions located in said at least one data sub-window.

18. (Rejected) The method of claim 17, wherein said estimated bit time is derived from said serialized stream of digital audio data.

19. (Rejected) The method of claim 18, and further comprising:

estimating minimum and maximum bit window times;

constructing a bit window from said minimum and maximum bit window times;

identifying transitions in said serialized stream of digital audio data which occur within said constructed bit window, the time separating a set of successive identified transitions being a measurement of said estimated bit time.

20. (Rejected) A bi-phase decoder for use in decoding a stream of AES-3 digital audio data, comprising:

a decoder circuit coupled to receive a stream of AES-3 digital audio data, an estimated bit time for said stream of AES-3 digital audio data and a fast clock, said fast clock having a frequency of about at least twenty times faster than a frequency of said stream of AES-3 digital audio data; and

a data store coupled to said decoder circuit, said data store receiving subframes of digital audio data extracted, from said stream of AES-3 digital audio data by said decoder circuit;

said decoder circuit extracting subframes of said digital audio data by constructing a timing window from said estimated bit time, sampling said stream of AES-3 digital audio data using said fast clock and applying said sampled stream of AES-3 digital audio data to said timing window to identify

transitions, in said sampled stream of AES-3 digital audio data, indicative of preambles of said subframes of digital audio data;

wherein said bit time is estimated by averaging a plurality of data stream pulse lengths and the time separating a first set of successive identified transitions is a first measurement of said estimated bit time.

21. (Rejected) The apparatus of claim 20, wherein said constructed timing window has a preamble sub-window and at least one data sub-window and wherein preambles of said subframes of digital audio data are indicated by a combination of at least one transition located in said preamble sub-window and at least one transition located in said at least one data sub-window.

22. (Rejected) The apparatus of claim 21, and further comprising a bit time estimator circuit having an input coupled to receive said stream of AES-3 digital audio data and an output coupled to said decoder circuit, said bit time estimator determining said estimated bit time for output to said decoder circuit.

23. (Rejected) A method of extracting digital audio data words from a serialized stream of digital audio data, comprising:

constructing a timing window from an estimated bit time for said serialized stream of digital audio data, said timing window having a preamble sub-window and at least one data sub-window;

extracting plural digital audio data words from said serialized stream of digital audio based upon the location of each transition in said serialized stream of digital audio data relative to said preamble sub-window and said at least one data sub-window of said timing window;

each one of said extracted plural digital audio data words having a preamble identifiable by a combination of at least one transition located in said preamble sub-window of said timing window and at least one transition located in said at least one data sub-window of said timing window;

estimating minimum and maximum bit window times;

constructing a bit window from said minimum and maximum bit window times;

identifying transitions in said serialized stream of digital audio data which occur within said constructed bit window, wherein the time separating a first set of successive identified transitions is a first measurement of said estimated bit time.

24. (Rejected) A method of extracting digital audio data words from a serialized stream of digital audio data, comprising:

constructing a timing window from an estimated bit time for said serialized stream of digital audio data, said timing window having a preamble sub-window and at least one data sub-window;

sampling said serialized stream of digital audio data at a fast sample rate; and

extracting plural digital audio data words from said serialized stream of digital audio based upon the location of each transition in said sampled stream of digital audio data relative to said preamble sub-window and said at least one data sub-window of said timing window;

estimating minimum and maximum bit window times;

constructing a bit window from said minimum and maximum bit window times;

identifying transitions in said serialized stream of digital audio data which occur within said constructed bit window, the time separating a set of successive identified transitions being a measurement of said estimated bit time; and

determining said estimated bit time from a running average of plural measurements of said estimated bit time.

9. <u>RELATED EVIDENCE APPENDIX</u>

None.

10. RELATED PROCEEDINGS APPENDIX

None